ETC/ECE 5.1 DIGITAL SIGNAL PROCESSING

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.1	Digital Signal Processing	3	1	2	3	100	25	25	--	--	150

Course Objectives:

The subject aims to provide the student with:

1. Ability to perform frequency domain analysis of LTI systems.
2. Ability to compute Discrete Fourier Transform and Fast Fourier Transform of a time domain signal.
3. Ability to design Infinite Impulse Response Filters and Finite Impulse Response filters.
4. An understanding of sampling rate conversion and its applications.

Course Outcomes:

The student after undergoing this course will be able to:

1. Perform frequency domain analysis of LTI systems.
2. Analyze phase response of LTI system.
3. Compute DFT and FFT of a signal.
4. Analyze the effect of causality in designing practical filters.
5. Explain the advantages and disadvantages of IIR and FIR Filter.
6. Design IIR Filter and FIR filter.
7. Explain the need and applications of sampling rate conversion.

UNIT - 1 (12 hours)

Sampling of continuous time signals: Periodic sampling; Frequency domain representation of sampling; Reconstruction of a band limited Signal from its samples; Discrete-time processing of Continuous time signals;
Continuous time processing of discrete time signals; changing the sampling rate using discrete time processing.
Transform analysis of LTI systems: Introduction, Frequency response of LTI systems, system functions for systems characterized by linear constant coefficient difference,
Frequency response for rational system functions, relationship between magnitude and phase, All-pass systems, minimum phase systems, Linear systems with generalized linear phase; systems with linear phase.

UNIT - 2 (12 hours)

The Discrete Fourier transform: Introduction, Representation of periodic sequences: The Discrete Fourier Series, Properties of the Discrete Fourier series, Fourier transform of periodic signals; sampling the Fourier transform, Discrete Fourier transform, Properties of Discrete Fourier Transform, Linear Convolution using the DFT. Computation of the Discrete Fourier transform, efficient computation of DFT, Decimation-in-time FFT (in-place computations), Decimation-in-frequency FFT (in-place computations).

UNIT - 3 (12 hours)

Structures for discrete-time systems: Block diagram representation of linear constant-coefficient difference equations; Signal flow graph representation; Basic structures of IIR systems: Direct, cascade, parallel; Transposed forms; Basic network structures for FIR systems: Direct Cascade, Structures for linear-phase FIR systems, causal generalized linear-phase systems.

Filter design techniques: Design of Discrete-time IIR filters from continuous-time filters; Filter design by impulse invariance, bilinear transformation, Examples of bilinear transformation design, Butterworth, Chebyshev filter design.

UNIT - 4 (12 hours)

Design of FIR filters by windowing: Properties of commonly used windows, incorporation of generalized linear phase, the Kaiser window filter design method
Examples of FIR filter design by the Kaiser Window methods
Optimum approximations of FIR filters; optimal type I low pass filters, optimum type II low pass filters. Characteristics of optimum FIR filters, Examples of equiripple approximation: lowpass filter.
Multirate Signal Processing: Interchange filtering and down sampling/up sampling; Polyphase decompositions; Polyphase implementation of decimation filters, Polyphase implementation of interpolation filters.

Recommended Readings:

1. A. V. Oppenheim, R. W. Schafer; Discrete-Time Signal Processing; Pearson
2. J. G. Proakis, D. G. Manolakis; Digital Signal Processing: Principles, Algorithms, and Applications ; Pearson
3. S Salivahanan; Digital Signal Processing, 3rd Ed.; McGraw Hill Education

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. To plot the magnitude and phase response of various signals.
2. To study the frequency response of second order resonator, notch filter, averaging filter, comb filter and allpass systems.
3. To observe the effect of a linear and non-linear phase response on signals.
4. To find and plot the DTFT of signals
5. To study the effect of linear and circular convolution on signal
6. To find and plot DFT of signal
7. To design a butterworth filter using impulse invariance method and bilnear transformation
8. To design a chebyshev filter using impulse invariance method and bilnear transformation
9. To deisgn a FIR filter using windowing
10. To deisgn a FIR filter using frequency sampling method.

ETC/ECE 5.2 TRANSMISSION LINES & ANTENNAS

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.2	Transmission Lines & Antennas	3	1	--	3	100	25	--	--	--	125

Course Objectives:

The subject aims to provide the student with:

1. An understanding of Transmission Lines under different Terminal Conditions.
2. An understanding of Transmission Lines at Radio Frequency and Matching of Transmission Lines under different loads.
3. An understanding of the Antenna Concepts and Parameters.
4. An understanding of Antenna Arrays and Analysis of Field Patterns.

Course Outcomes:

The student after undergoing this course will be able to:

1. Analyze the working of Transmission Lines under different Terminal Conditions.
2. Analyze the Transmission Lines at Radio Frequency.
3. Estimate proper Matching of Transmission Lines using Smith Chart.
4. Analyze the working of different types of antennas.
5. Compute radiation pattern and Directivity for different types of field Patterns.

UNIT - 1 (12 hours)

Transmission-Line Theory: A line of cascaded T-sections (line constants: Z, Y, characteristic impedance Z_o, propagation constant).

The transmission line-general solution; physical significance of the equations, infinite line, Wavelength, velocity of propagation.

The distortion less line, Reflection on a line not terminated in Z_o (Voltage and current-phasors), Reflection coefficient, Input and transfer impedance, Open- and short-circuited lines.

UNIT - 2 (12 hours)

The Line At Radio Frequencies: Introduction, Constants for the line of zero dissipation (Lossless Lines), Voltages and currents on the dissipation less line (Voltage and Current phasors on the line for various terminations);

Standing waves, nodes, standing wave ratio (SWR), Directional Coupler.

Input-impedance of the dissipation less line: Input impedance of open- and short circuited lines, Power and Impedance measurement on lines, Reflection losses on the unmatched line.
The quarter-wave line, half-wave line, eighth-wave line.
The Smith circle diagram, Applications of the Smith chart; matching with the Smith chart.

UNIT - 3 (12 hours)

Basic Antenna Concepts: Antenna Parameters, Antenna Aperture and Aperture Efficiency, Effective Height, Maximum Effective Aperture of a Short Dipole and a Linear Half-Wave Antenna, Friss transmission formula.
Point Sources, Power patterns, Power theorem, radiation intensity, different power patterns (Unidirectional and bi-directional cosine, sine, sine-squared, cosine squared and (cosine) ^{n}.
The short electric dipole: Retarded vector potential, fields and radiation resistance, Radiation resistance of a half wave dipole and half wave antennas.

UNIT - 4 (12 hours)

Various forms of Antenna arrays, Arrays of point sources: Isotropic point sources of: (i) same amplitude and phase (ii) same amplitude but opposite phase (iii) same amplitude and in phase quadrature (iv) equal amplitude and any phase (v) unequal amplitude and any phase.
Patterns multiplication: Radiation pattern of four and eight isotropic elements fed in phase.
Linear array: Linear array with n isotropic point sources with equal amplitude and spacing; Broadside case; End-fire case, End fire array with increased directivity, scanning array.
Loop antenna: Field of a small loop, field pattern of circular and square loop
Helical Antenna: Geometry, Transmission and radiation modes, Practical design considerations.
Construction and Characteristics of: Horn antennas (Rectangular and Conical), Reflector antennas: Corner, paraboloidal, Cassegrain feed, Lens antennas, Yagi-Uda array, V- and Rhombic-antenna.
Patch or Microstrip Antennas, Rectangular patch, square patch.

Recommended Readings:

1. J.D. Ryder; Networks, Lines and Fields; PHI.
2. J.D. Kraus; Antennas and Wave Propagation; McGraw Hill Education.
3. K. D. Prasad; Antenna & Wave Propagation; Satya Prakashan
4. E.C. Jordan, K. G. Balmain; Electromagnetic Waves & Radiating Systems; PHI.
5. George Kennedy; Electronic Communication Systems, 3rd Edition; Tata McGraw Hill
6. Ramo & Whinnery; Fields and Waves in Communication Circuits; John Wiley & Sons.

ETC/ECE 5.3 CONTROL SYSTEMS ENGINEERING

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.3	Control Systems Engineering	3	1	--	3	100	25	--	--	--	125

Course Objectives:

The subject aims to provide the student with:

1. An understanding of basic control system components, signal flow graphs and transfer functions.
2. An ability to evaluate stability of any given system model.
3. An ability to perform frequency domain stability analysis.
4. An ability to design compensators and controllers for a given application.

Course Outcomes:

The student after undergoing this course will be able to:

1. Differentiate between open and close loop system.
2. Analyze the signal flow graph and models representing systems and determine its transfer function.
3. Compute transient and steady state response of stable control systems.
4. Predict the stability of system by using root locus and Routh-Hurwitz criteria.
5. Predict the stability of system by using Nyquist criterion, bode plot and polar plot.
6. Analyze the systems using state space variables.
7. Design a compensator in time domain and in frequency domain.
8. Select appropriate controller for a given control application.

UNIT - 1 (12 hours)

Introduction to control systems: Types of control systems, Examples of Control systems, basic concept of open-loop and closed-loop control systems;

Mathematical modeling and representation of mechanical (translational & rotational) and electrical systems.

Conversion of mechanical to analogous electrical systems (force-voltage and force- current analogy);

Block diagrams; Signal flow graphs and transfer functions.

UNIT - 2 (12 hours)

Standard Test Inputs, Transient response of first and second order systems; Type -0, -1 and –2 control systems. Steady state error and error co-efficient; Effects of proportional, derivative and integral systems.

Stability: Stability concept, Routh-Hurwitz criteria; Root-locus techniques**.**

UNIT - 3 (12 hours)

State space variable Analysis: Concept of state, state variable and state model. State space representation of continuous time LTI system.

Frequency-domain analysis: Correlation between time and frequency response, Polar-plots, Bode-plots, Nyquist-plots; Relative stability using Nyquist-plot.

UNIT - 4 (12 hours)

Compensators: Concept of compensators; types of compensators; Design of Cascade compensator in time domain- Lead, Lag and Lead-Lag compensation;

Design of Cascade compensator in frequency; domain -Lead, Lag and Lead-Lag compensation.

Introduction to Controllers: PI, PD and PID controllers**.** Ziegler–Nichols rules for tuning PID Controllers.

Recommended Readings:

1. M. Gopal; Control Systems-Principles and Design; Tata Mc Graw Hill
2. K. Ogata; Modern Control Engineering; PHI
3. I. J. Nagrath and M. Gopal; Control Systems Engineering; The New Age International
4. A. Nagoor Kani; Control Systems; RBA Publications, Chennai
5. D. Roy Choudhry; Modern Control Engineering; PHI
6. Salivahanan S.; Control Systems Engineering; Pearson Education

ETC/ECE 5.4 EMBEDDED SYSTEMS

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.4	Embedded Systems	3	1	2	3	100	25	--	--	25	150

Course Objectives:

The subject aims to provide the student with:

1. An understanding of architecture and programming of 8051 microcontroller.
2. An ability to interface external devices with 8051.
3. An understanding of architecture and programming of PIC18 microcontroller.
4. An ability to interface external devices with PIC18.

Course Outcomes:

The student after undergoing this course will be able to:

1. Describe the features of 8051 and PIC18 microcontroller.
2. Select appropriate microcontroller for different applications.
3. Interface microcontroller with hardware for a given application.
4. Write and execute assembly language programs for a given application.
5. Design and implement microcontroller based applications.

UNIT - 1 (12 hours)

8051 architecture: Overview of 8051 Family, Data types and directives , Flag bits, PSW register, Register banks and stacks, Addressing modes, Assembly language programming ,JUMP ,LOOP and CALL instructions, Arithmetic instructions, Logic instruction ,Bit instructions , I/O port programming , Bit manipulation instructions.

UNIT - 2 (12 hours)

Interrupts and Interfacing: Timer/Counter basics and programming , Serial communication basics and programming , 8051 connection to RS232, basics of interrupts and programming timer interrupts, external hardware interrupts and serial communication interrupts, Interrupt Priority , Interfacing of LCD,ADC, Stepper motor, Keyboard, DAC and External memory to 8051 .

UNIT - 3 (12 hours)

PIC 18 Architecture: Block diagram, WREG, PIC File Register, Using Instructions with the default Access bank, PIC Status Register, PIC Data Format & Directives, Introduction to PIC Assembly language Programming, The Program Counter and Program ROM space in the PIC, Harvard and RISC Architecture in the PIC, Branch Instructions & Looping, Call Instructions & Stack, PIC 18 Time Delay and Instruction Pipeline, PIC I/O Port programming, I/O Bit Manipulation Programming.

UNIT - 4 (12 hours)

Arithmetic, Logic Instructions and Programs, Bank Switching: Addressing Modes, Look-up Table and Table Processing. PIC 18 Timer Programming in Assembly: Programming Timers 0,1,2 and 3, Counter Programming, Timers 2 & 3,PIC 18 Serial Programming in Assembly, PIC18 Interrupts, Interrupt Programming in Assembly, PortB-Change Interrupt, CCP Programming: Compare Mode Programming, Capture Mode Programming, PWM Programming, SPI Bus Protocol.

Recommended Readings:

1. Muhammad Ali Mazidi, Janice Gillispie Mazidi; The 8051 Microcontroller and Embedded systems; Pearson Education
2. Muhammad Ali Mazidi, Rolind D. Mckinlay, Danny Causey; PIC Microcontroller and Embedded Systems Using Assembly & C for PIC18; Pearson Education
3. Kenneth J. Ayala; The 8051 Microcontroller, Architecture, Programming & applications, second edition; Penram International.
4. Barry B. Brey; Applying PIC18 Microcontrollers: Architecture, Programming, and Interfacing using C and Assembly; Prentice Hall

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1) Using 8051
   - i. Basic Programs
   - ii. Using Branch Instructions
   - iii. Using Call Instructions
   - iv. Generating Time delays
   - v. I/O Programming
   - vi. Timer Programming
   - vii. Serial Port Programming
   - viii. Interrupt programming
2) Using PIC 18
   - i. Basic Programs
   - ii. Using Branch Instructions
   - iii. Using Call Instructions

iv. Generating Time delays
v. I/O Programming
vi. Timer Programming
vii. Serial Port Programming
viii. Interrupt programming

ETC/ECE 5.5 VLSI DESIGN AND TECHNOLOGY

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.5	VLSI Design And Technology	4	--	2	3	100	25	--	--	25	150

Course Objectives:

The subject aims to provide the student with:

1. An in depth knowledge of the MOSFET operation and the ability to derive the threshold voltage & current equations.
2. An understanding of the theory of CMOS Inverter and Switching characteristics and the capability to write SPICE programs for various circuits.
3. The capability to design combinational circuits in CMOS logic and draw Layouts for the same and design circuits using VHDL.
4. An understanding of the various processes involved in VLSI technology and chip fabrication and the various methods of testing circuits.

Course Outcomes:

The student after undergoing this course will be able to:

1. Calculate the threshold voltage for a given MOSFET and obtain the value of Drain current for any given biasing condition.
2. Analyze the effects of narrow channel and short channel on device characteristics.
3. Calculate the voltage parameters and noise margin of a CMOS Inverter and also explain its switching characteristics.
4. Write the SPICE program for modeling MOSFET circuits.
5. Implement complex combinational functions in CMOS logic and draw the Layout for the same.
6. Design simple Combinational and Sequential circuits using VHDL.
7. Explain the various MOSFET fabrication processes and explain the Design for Testability methods.
8. Compute the Test pattern which will detect faults in a given circuit.

UNIT - 1 (16 hours)

MOS transistors: Structures, MOS system under external bias, operation of MOS transistor (MOSFET),

MOS transistors: Threshold voltage MOSFET current-voltage characteristics (CGA), channel length modulation, substrate bias effect.

Measurements of parameters – KN, VTP & γ. Short channel effects, Narrow channel effects. Latch up and its prevention. MOSFET capacitances.

UNIT - 2 (16 hours)

Modeling of MOS transistor circuits using SPICE. (Level 1 model equations).
MOS Inverters: Static load MOS Inverters.
CMOS inverter design: operation, DC characteristics, calculation of VIL, VIH, VTH, VOH and VOL. Noise margins power and area considerations.
Switching Circuit Characteristics: Rise, fall and delay time, gate delays, transistor sizing, static and dynamic power dissipations CMOS logic gate design: Fan in and fan out.

UNIT - 3 (16 hours)

MOS transistor switches: CMOS logic- Inverter, NOR, NAND and combinational logic, Compound gates, Multiplexers, Transmission gates, Latches and Registers.
Implementation of Boolean Expressions using transmission gates and CMOS logic.
NOR, NAND layouts (Euler paths).
Complex logic gates and their layouts (Euler paths),
MOSIS layout design rules (full-custom mask layout designs), stick diagrams. Layout editors (Magic/Micro Wind) and circuit extraction.
Introduction to VHDL language. VHDL Programs and test benches for Adder, Subtractor, Decoder, Encoder, Multiplexer, Demultiplexer, Flip Flops, Registers and Counters.

UNIT - 4 (16 hours)

Silicon semiconductor technology: Wafer processing, oxidation, epitaxy, deposition, etching, Photo-Lithography, Ion-implantation and diffusion. Silicon gate process. Chemical Vapor Deposition.
Basic CMOS technology: n-well and p-well CMOS process. Silicon on insulator
Testing: Test procedure, Design for Testability (DFT) Scan – Based test, Boundary- Scan design, Built in self-test (BIST).Automatic Test-Pattern generation (ATPG), fault models, fault simulation.

Recommended Readings:

1. Sung-Mo (Steve) Kang , Yusuf Leblebici; CMOS Digital Integrated Circuits Analysis & Design; McGraw-Hill Education
2. Neil Weste, David Harris; CMOS VLSI Design: A Circuits and Systems Perspective; Pearson
3. Jan M. Rabaey; Digital Integrated Circuits – A Design perspective; Pearson Education
4. Bhaskar; VHDL Primer; PHI
5. Stephen Brown, Zvonco Vranesic; Fundamentals of Digital logic with VHDL design; McGraw-Hill Education
6. Wayne Wolf; Modern VLSI design (Systems on Silicon); PHI

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. SPICE program for Inverter VTC.
2. SPICE program for parameter measurement KN, VTP & γ.
3. SPICE program for NAND gate.
4. SPICE program for NOR gate.
5. SPICE program for channel length modulation effect.
6. SPICE program for Transmission Gate.
7. VHDL programs for Combinational circuits.
8. VHDL programs for sequential circuits.
9. MAGIC layout for Inverter and parameter extraction in SPICE.
10. MAGIC layout for NAND and parameter extraction in SPICE.
11. MAGIC layout for XOR and parameter extraction in SPICE.
12. MAGIC layout for XNOR and parameter extraction in SPICE.
13. MAGIC layout for Boolean function f = ((A+B)(C+D)) 'and parameter extraction in SPICE .
14. MAGIC layout for Boolean function f=((AB)+(CD)) 'and parameter extraction in SPICE
15. MAGIC layout for 2x1 MUX in Transmission Gates.

ETC/ECE 5.6 ANALOG COMMUNICATION

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 5.6	Analog Communication	4	--	2	3	100	25	--	25	--	150

Course Objectives:

The subject aims to provide the student with:

1. An understanding of basic analog communication systems and their components.
2. An ability to solve problems related to design of analog modulation schemes.
3. The capability to design simple analog modulation systems.
4. An understanding of effect of noise on analog communication systems.

Course Outcomes:

The student after undergoing this course will be able to:

1. Assess and calculate key frequency and time domain design parameters for analog modulation schemes.
2. Design block level and circuit level systems for analog modulation and demodulation.
3. Quantitatively assess the impact of noise in analog communication systems.
4. Design block-level systems for super heterodyne receiver with auxiliary circuits and pulse modulation and demodulation circuits.

UNIT - 1 (16 hours)

Amplitude modulation: DSB-FC, DSB-SC, SSB, modulation and demodulation. Spectrum, power and efficiency. Implementation of amplitude modulators and demodulators. DSBSC-Balanced modulator, coherent detection of DSBSC, squaring loop detection. SSB-SC- Phase Shift and Third method of generation. Coherent detection of SSBSC.

Carrier acquisition – Phase locked loop, in DSB-SC and in SSB-SC. Signal multiplexing: FDM and TDM. AM Broadcasting: Radio transmitter and Receiver.

UNIT - 2 (16 hours)

Angle modulation: FM and PM signals, Relationship between frequency and phase modulation. Tone modulated FM. Arbitrary modulated FM. Spectrum of FM and PM, Implementation of angle modulators and demodulators: Direct method using FET, Armstrong method of generation. Slope detector, Foster-Seelay Discriminator, Ratio detector. FM broadcasting, FM stereo broadcasting.

UNIT - 3 (16 hours)

Sources of Noise: Shot noise, resistor noise. Calculation of noise in linear systems. Noise bandwidth. Noise temperature, Noise figure, measurement of noise figure. Narrowband noise.
Effect of noise in DSB-SC, Effect of noise in SSB-SC.
Noise in FM: AM FM receiving system, calculation of SNR, comparison of AM and FM, pre-emphasis and de-emphasis. Noise in phase modulation.

UNIT - 4 (16 hours)

Pulse modulation schemes: PAM, PPM and PWM, Generation and detection.
Transmitter and Receiver systems: AM and FM modulation and demodulation circuits, AM and FM transmitter receiver circuits, The phase locked loop. TRF and super heterodyne receivers, solid state circuits and design considerations for RF amplifiers, mixers, IF amplifiers, AGC, AFC, Amplitude limiter.

Recommended Readings:

1. George Kennedy; Electronic Communication Systems; Tata McGraw Hill
2. John G. Proakis , Masoud Salehi; Fundamentals of Communication Systems, 2nd Ed.; Pearson Education
3. Wayne Tomasi; Electronic Communications systems, 3rd Ed.; Pearson Education
4. Upamanyu Madhow; Introduction to Communication Systems; Cambridge University Press
5. R. P. Singh, S. Sapre; Communication systems: Analog and Digital, 3rd Ed.; Tata McGraw Hill
6. Dennis Roddy, John Coolen; Electronic communication system, 4th Ed.; Pearson Education
7. Simon Haykin; An Introduction To Analog And Digital Communications; John Wiley & Sons
8. Taub, Schilling, Saha; Principles of communication systems, 3rd Ed.; Tata McGraw Hill

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. DSB-FC AM Generation and demodulation
2. DSB-SC Generation and Demodulation
3. SSB AM Generation and Demodulation
4. FM generation and demodulation
5. AM/FM transmission and reception
6. RF amplifiers, mixers and IF amplifiers
7. PAM, PWM, PPM generation and detection
8. Effect of Noise in DSB-FC
9. Effect of Noise in DSB-SC
10. Effect of Noise in SSB
11. Effect of Noise in FM
12. AGC/AFC

ETC/ECE 6.1 ELECTRONIC SYSTEM DESIGN AND MANUFACTURING

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 6.1	Electronic System Design and Manufacturing	4	--	2	3	100	25	25	--	--	150

Course Objectives:

The subject aims to provide the student with:

1. An introduction to the interference in electronic circuits.
2. An understanding of the effect of shield on circuits and filtering circuits for electronic systems.
3. An introduction to EMC compliance of passive components.
4. An understanding noise sources and their effects on electronic circuits and systems.
5. An understanding of rules for PCB layout.

Course Outcomes:

The student after undergoing this course will be able to:

1. Explain EMC regulations for military and commercial standards.
2. Design shielding circuits to prevent capacitive and inductive coupling.
3. Design filtering circuits for electronic systems.
4. Explain EMC compliance of capacitor and conductor.
5. Calculate S/N ratio and noise factor for various electronic circuits.
6. Explain ESD protection in equipment design.
7. Explain procedure for PCB layout and stackup.

UNIT - 1 (16 hours)

Electromagnetic Compatibility: Introduction, Noise and Interference, Designing for Electromagnetic Compatibility, Engineering Documentation and EMC, United States' EMC Regulations, European Union's EMC Requirements, Military Standards.

Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables.

Grounding of Electronic Systems: Signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds.

UNIT - 2 (16 hours)

Balancing & Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, and system bandwidth.

EMC Compliance of Passive Components: Capacitors: Electrolytic Capacitors, Film Capacitors, Mica and Ceramic Capacitors, Feed-Through Capacitors, Paralleling Capacitors. Conductors: Inductance and resistance of Round and Rectangular Conductors.

UNIT - 3 (16 hours)

Intrinsic Noise Sources: Thermal Noise- Characteristics, Equivalent Noise Bandwidth, Shot Noise, Contact Noise, Popcorn Noise, Addition of Noise Voltages, Measuring Random Noise.

Active Device Noise: Noise Factor, Measurement of Noise Factor - Single-Frequency Method, Noise Diode Method, Calculating S/N Ratio and Input Noise Voltage from Noise Factor, Noise Voltage and Current Model, Measurement of V_n and I_n , Calculating Noise Factor and S/N Ratio from V_n–I_n, Optimum Source Resistance, Noise Factor of Cascaded Stages, Noise Temperature

Bipolar Transistor Noise: Transistor Noise Factor, V_n–I_n for Transistors.
Field-Effect Transistor Noise: FET Noise Factor, V_n–I_n Representation of FET Noise.
Noise in Operational Amplifiers: Methods of specifying Op-Amp Noise, Op-Amp Noise Factor.

UNIT - 4 (16 hours)

Protection Against Electrostatic Discharges (ESD): Static generation, human body model, static discharge, ESD protection in equipment design.

PCB Layout and Stackup: General PCB layout considerations: Partitioning, Keep out zones, critical signals, and system clocks. PCB-to-Chassis ground connection.
Return Path Discontinuities: Slots in Ground/Power Planes, Split Ground/Power Planes. PCB Layer stackup: One- and Two-Layer boards, multilayer boards, general PCB design procedure.

Recommended Readings:

1. Henry W. Ott; Electromagnetic Compatibility Engineering; John Wiley & Sons.
2. W Bosshart; Printed Circuit Boards - Design & Technology, 1st Edition; Tata McGraw Hill
3. Clayton R. Paul; Introduction to Electromagnetic Compatibility, 2nd Edition; Wiley.
4. Chetan Kathalay; A Practical Approach to Electromagnetic Compatibility -With Introduction to CE Marking (EMC SERIES), 2nd Ed.; EMC Publications.
5. Mark I. Montrose; Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers, 2nd Ed.; Wiley
6. Howard W. Johnson, Martin Graham; High Speed Digital Design: A Handbook of Black Magic,1st Ed. ; Pearson Education

Term Work:

Term work shall consist of following assignments (or related work)

1. Noise and Interference.
2. United States' EMC Regulations.
3. European Union's EMC Requirements.
4. Inductive coupling.
5. Capacitive coupling.
6. Capacitors.
7. Conductors.
8. Intrinsic Noise Sources.
9. Noise Factor.
10. Transistor Noise Factor.
11. FET Noise Factor.
12. Static discharge.
13. ESD protection in equipment design.
14. Multilayer Boards.
15. General PCB Design Procedure.

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. Selection of a mini project.
2. Understanding Datasheet of the components.
3. Soldering.
4. Schematic Design.
5. Layout Design.
6. Fabrication of PCB.
7. Component mounting and soldering on PCB.
8. Inspection and testing of PCB.
9. Calibration.
10. Rework/ Repairs.

ETC/ECE 6.2 HIGH PERFORMANCE COMPUTING ARCHITECTURES

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 6.2	High Performance Computing Architectures	4	--	2	3	100	25	--	--	--	125

Course Objectives:

The subject aims to provide the student with:

1. An ability to write Verilog Hardware Descriptor Language programs.
2. An ability to program FPGA's with Verilog.
3. A detailed introduction to general purpose graphical processing units.
4. An ability to write CUDA programs for performing matrix multiplication.

Course Outcomes:

The student after undergoing this course will be able to:

1. Write programs to design circuits using Verilog Hardware Description Language.
2. Explain in detail the architecture of popular High Performance FPGA's.
3. Implement and test digital circuits on FPGAs.
4. Explain the key features and advantages of parallel computation.
5. Explain the architecture of GPU's and GPGPUs.
6. Write CUDA programs for performing Matrix Multiplication.

UNIT - 1 (16 hours)

Hardware Descriptor Languages: Emergence of HDLs, Design Flow using HDLs, Importance of HDLs.
Hierarchical Modeling Concepts: Modules, Instances.
Data Types: Nets, Registers, Vectors, Arrays, Integer, Real, and Time, Memories, Parameters, Strings. Modules and Ports.
Gate Level Modeling: Design of Ripple Carry Adder, Shift Register using DFF, Multiplexer, Demultiplexer, Decoder, Encoder.

UNIT - 2 (16 hours)

Dataflow Modeling: Continuous assignment (assign) statement, assignment delay, implicit assignment delay, and net declaration delay for continuous assignment statements.
Define expressions, operators, and operands. Operator types for all possible operations—arithmetic, logical, relational, equality, bitwise, reduction, shift, concatenation, and conditional.

Behavioral Modeling: Structured procedures, always and initial. Blocking and non-blocking procedural assignments. Conditional statements using if and else. Multiway branching, using case, casex, and casez statements, Looping statements such as while, for, repeat, and forever. Definition of sequential and parallel blocks.

UNIT - 3 (16 hours)

Tasks and functions in Verilog, Finite State Machine using Verilog.
Examples of design using Verilog HDL.
FPGA's: Design Flow for Designing with FPGA, Design simulation, Design synthesis,
Key Architecture features of high performance FPGAs: Xilinx Virtex 5, VIRTEX II Pro and VIRTEX 4 with PowerPC and Altera Cyclone FPGA with NIOS II.
Implementation of Hardware Multiplier, ALU, Adder/Subtractor on FPGA.

UNIT - 4 (16 hours)

Introduction to GPU: GPUs as Parallel Computers, Architecture of a modern GPU, Why More Speed or Parallelism, Parallel Programming Languages and Models Overarching Goals, Evolution of Graphics Pipelines; the Era of Fixed-Function Graphics Pipelines, Evolution of Programmable Real-Time Graphics, Unified Graphics and Computing Processors, GPGPU, An Intermediate Step, GPU Computing Scalable GPUs Recent Developments, Future Trends.
Introduction to CUDA: Data Parallelism CUDA Program Structure, a Matrix-Matrix Multiplication Example.

Recommended Reading:

1. S. Palnitkar; Verilog HDL: A Guide to Digital Design and Synthesis; Prentice Hall
2. J. Bhasker; Verilog HDL Synthesis - A Practical Primer; Star Galaxy Publishing
3. David B Kirk, Wen Mei W Hwu; Programming Massively Parallel Processors: A Hands- On Approach; Elsevier India Private Limited
4. Ananth Grama, Anshul Gupta, George Karypis, Vipin Kumar; Introduction to Parallel Computing, 2nd Ed.; Pearson Education

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. Verilog Program for Full Adder
2. Verilog Program for Ripple Carry Adder using Gate Level Modeling
3. Verilog Program for MUX/DEMUX using DataFlow Modeling
4. Verilog Program for DECODER/ENCODER
5. Verilog Program for JKFF/SRFF/DFF/TFF
6. Verilog Program for UP/Down Counter using Behavioral Modeling
7. Verilog Program for FSM
8. Verilog Program for RAM
9. Verilog Program for Shift Register.
10. ALU on Xilinx/Altera FPGA
11. Hardware Multiplier on Xilinx/Altera FPGA.
12. Counter on FPGA
13. Fast Fourier Transform (FFT) Calculation using Verilog.
14. CUDA program for Matrix Multiplication.

ETC 6.3 DIGITAL COMMUNICATION

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC 6.3	Digital Communication	3	1	--	3	100	25	--	25	--	150

Course Objectives:

The subject aims to provide the student with:

1. An introduction to digital modulation systems, the underlying mathematical models and the process of converting analog signal to digital.
2. An ability to analyze digital modulation schemes on different performance metrics.
3. An understanding of requirements and issues for optimal receiver design for digital signals.
4. An overview of traffic engineering and different telecommunication switching systems.

Course Outcomes:

The student after undergoing this course will be able to:

1. Evaluate the benefits of digital modulation schemes over analog for a given application.
2. Explain Phase/amplitude/frequency shift keying and quadrature amplitude modulation techniques.
3. Analyze the performance of baseband digital modulation techniques in terms of error rate and spectral efficiency.
4. Select the blocks in design of digital communication system for error and interference free communication.
5. Explain OFDM scheme and implement using FFT.
6. Explain different telecommunication switching systems.
7. Calculate traffic capacity and blocking probability for given performance parameters.

UNIT - 1 (12 hours)

Introduction to digital communication: Analog communication v/s Digital Communication, Elements of digital communication system, Communication channels and their characteristics.

Mathematical models for communication channels: Additive noise channel, linear filter channel, linear time variant filter channel.

Sampling: Sampling Theorem, Natural Sampling, Flat-top sampling, Signal Recovery through holding, Equalization.

Digital Representation of Analog Signal: Quantization of Signals, Quantization Error, Mid-rise & Mid-tread quantizers, Uniform & Non-uniform quantizers, Companding- μ-Law and A-Law.

Pulse digital modulation techniques: Pulse code modulation, Line coding, Differential Pulse Code Modulation, Delta modulation, Adaptive delta modulation.

UNIT - 2 (12 hours)

Digital modulation and transmission:
Phase shift keying: Binary Phase Shift Keying, Differential Phase Shift Keying, Differential Encoded Phase Shift Keying, Quadrature Phase Shift Keying, M-ary Phase Shift Keying
Frequency Shift Keying: Binary Frequency Shift Keying, M-ary Frequency Shift Keying, Minimum Shift Keying. Gaussian Minimum Shift Keying.
Amplitude Shift keying: Quadrature Amplitude Shift Keying.
Quadrature Amplitude-Modulated Digital Signals: Geometric Representation of QAM Signals, Demodulation and Detection of QAM Signals, Probability of Error for QAM
Pulse shaping to reduce Inter-channel and Inter-symbol interference: Duobinary Encoding, Nyquist criterion, Regenerative repeater.

UNIT - 3 (12 hours)

Optimal reception of digital signal: A baseband signal receiver: Peak Signal to RMS Noise Output Voltage Ratio, Probability of Error. Optimum Threshold: Maximum Likelihood Detector and Bayes Receiver, probability of error.

Optimum receiver for both baseband and passband: Calculation of Optimum Filter transfer function, Optimum Filter realization using Matched Filter, probability of error of the Matched Filter, Optimum Filter realization using Correlator.

Optimal coherent reception: PSK, FSK and QPSK, Signal space representation and probability of error. Comparison of modulation systems.

Multicarrier Modulation and OFDM: Orthogonal Frequency-Division Multiplexing, Modulation and Demodulation in an OFDM System, An OFDM System implemented via the FFT Algorithm, Spectral characteristics of OFDM Signals, Peak-to-Average power ratio in OFDM Systems, Applications of OFDM.

UNIT - 4 (12 hours)

Switching Systems: Classification of switching systems, simple telephone communication, Basics of a switching system, signaling tones, principles of common control, touch tone dial telephone, Centralized SPC and Distributed SPC.
Time Division Switching: Basic Time Division Space Switching, Basic Time Division Time Switching, Time multiplexed Space Switching, Time Multiplexed Time Switching.
Traffic Engineering: Network Traffic Load & Parameters, Grade of Service & Blocking Probability, Incoming Traffic & Service Time Characterization.

Recommended Readings:

1. John G Proakis, Masoud Salehi; Fundamentals of Communication Systems, 2nd Ed.; Pearson Education
2. K Vishwanathan; Telecommunication Switching Systems & Networks, 2nd Ed; Prentice Hall of India.
3. Taub, Schilling, Saha; Principles of Communication Systems, 3rd Edition, Tata McGraw Hill Publishing Company.
4. R. P. Singh, S. Sapre; Communication systems: Analog and Digital, 3rd Ed.; Tata McGraw Hill
5. Bernard Sklar; Digital Communications : Fundamental & Applications, 2nd Edition; Pearson Education
6. Simon Haykins; Communication Systems, 3rd Edition, John Wiley & Sons.
7. K. Sam Shanmughan; Digital and Analog Communication Systems; John Wiley & Sons Pvt.

ETC/ECE 6.4 INDUSTRIAL AUTOMATION AND INSTRUMENTATION

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 6.4	Industrial Automation and Instrumentation	3	1	2	3	100	25	--	--	25	150

Course Objectives:

The subject aims to provide the student with:

1. An understanding of the principle and working of the Data acquisition systems, CRO and different types of transducers.
2. Introduction to Virtual Instrumentation using LABVIEW.
3. Introduction to the automation systems using the programmable logic controllers.
4. An understanding of the different types of industrial interfacing standards.

Course Outcomes:

The student after undergoing this course will be able to:

1. Explain the principle and working of the CRO, DSO and Data acquisition systems.
2. Design and simulate virtual instruments for sensors and data acquisition using appropriate software.
3. Evaluate between different types of transducers for a given application.
4. Design and simulate various industrial control applications using the programmable logic controllers.
5. Explain the different types of industrial communication standards.

UNIT - 1 (12 hours)

Electronic Voltmeter: Non-integrating type: Ramp type, Staircase Ramp, Continuous balance, Successive Approximation. Integrating type: Potentiometer Integrating, Dual Slope Integrating Voltmeter. Sensitivity & Resolution of a DVM.

Oscilloscope: Block diagram, Classification of CROs, CRT control circuits, delay lines, multiple trace CRO, Time base circuits, synchronizing circuits, Digital storage oscilloscope. CRO probes: Active & Passive probes, Compensation for probes.

Virtual Instrumentation: Historical perspective, advantages, block diagram, Virtual instruments examples, the front panel, Sub VIs.

Data Acquisition systems (DAS): Basic block diagram of DAS, objective of DAS, Components of a DAQ system, types of signals, signal conditioning of inputs, importance of

instrumentation and isolation amplifier, Signal grounding and measurements, DAQ hardware configuration, Digital and Analog I/O considerations.

UNIT - 2 (12 hours)

Temperature Measurement Transducers: Resistance Temperature Detectors, Thermistors, Thermocouples.
Displacement Transducers: Basic displacement measurement scheme, different types of displacement transducers: Strain Gauge, Linear Variable Differential Transformer, Capacitive, Inductive, Piezoelectric, and Potentiometer.
Pressure Transducers: Inductive, Resistive and Capacitive transducers for measuring pressure.
Velocity Transducers: Basic principle of measuring velocity, Tachogenerator.
Flow measurement transducers: Turbo magnetic Flow meter, Electromagnetic Flow meter.
Optical transducers: Photoresistor, Photodiode, Phototransistor.

UNIT - 3 (12 hours)

Programmable Logic Controllers (PLC): PLC Advantages & Disadvantages, Overall PLC System, CPU & Programmable Monitors, PLC input & Output Modules (Interfaces).
General PLC Programming Procedure: Proper Construction of PLC Ladder diagrams, Process Scanning considerations.
Basic PLC Programming: Programming ON-OFF inputs to produce ON-OFF outputs, Concepts of latching, interlocking, jogging outputs via ladder programming.
PLC Timer Functions: PLC timer functions, Examples of timers and Industrial process timing applications.
PLC Counter functions: PLC Counters, Examples of Counter Functions, Industrial applications.
PLC data handling instructions: Move, Conditional Jump, Call Subroutine instructions.
Selecting a PLC: Factors to be considered while selecting a PLC.

UNIT - 4 (12 hours)

SCADA systems: Introduction and brief history of SCADA, Modern SCADA systems, SCADA software, Remote terminal units.
Data logger basics, Advantages of data loggers, anatomy of a data logger, types of data loggers, factors to be considered in selecting a datalogger.
Basic standards: RS-232 and RS-485, Electrical signal characteristics, Interface mechanical characteristics, Functional description of the interchange circuits.
Modbus: General overview, Modbus protocol structure.
Fieldbus: Introduction, General Fieldbus architecture, Basic requirements of Fieldbus standard.

Recommended Readings:

1. H. S. Kalsi; Electronic Instrumentation; Tata McGraw Hill.
2. Robert H. Bishop; Learning with LABVIEW 7 Express; Pearson Education.
3. John Webb, Ronal Weiss; Programmable Logic Controllers: Principles & Applications, 5th Edition; Prentice Hall of India.
4. Deon Reynders , Steve Mackay , Edwin Wright; Practical Industrial Data Communications: Best Practice Techniques; Newnes , An imprint of Elsevier
5. Clarke, G., Reynders, D., Wright, E.; Practical Modern SCADA Protocols DNP3, 60870.5 and Related Systems, 1st Edition, Newnes , An imprint of Elsevier

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. Fault simulation using CRO trainer
2. Virtual Instruments ,Sub VIS
3. Loops using LABVIEW
4. Structures using LABVIEW
5. Arrays and Clusters using LABVIEW
6. Displacement Transducers
7. Pressure Transducers
8. Flow Transducers
9. Temperature Transducers
10. Data Acquisition using LABVIEW
11. Ladder program to implement latching, interlocking.
12. Ladder program to implement jogging.
13. Ladder program to implement timing applications.
14. Ladder program to implement counting applications
15. Ladder program to implement data handling instructions
16. Implement any of the above ladder programs using the SCADA software.

ETC/ECE 6.5 OPERATING SYSTEMS

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 6.5	Operating Systems	3	1	--	3	100	25	--	--	--	125

Course Objectives:

The subject aims to provide the student with:

1. An ability to describe control structures and techniques used in a typical operating system for process management.
2. The knowledge of approaches to deal with deadlocks and mechanisms to ensure the orderly execution of processes to maintain data consistency.
3. An ability to describe ways to manage memory, and implement virtual memory.
4. A general understanding of file management aspects of an operating system and various disk scheduling policies.
5. A capability to describe the implementation of OS concepts in Linux.

Course Outcomes:

The student after undergoing this course will be able to:

1. Summarize the objectives of an Operating System.
2. Compare multiprocessor, multiprogramming and time sharing systems.
3. Draw Gantt chart and calculate the waiting time for a given set of processes, for various CPU scheduling algorithm.
4. Write pseudo codes to solve the classic problems of Process Synchronization.
5. Solve problems related to Resource Allocation in case of Deadlocks.
6. Enlist the advantages and disadvantages of various memory management strategies.
7. Illustrate the page replacement Algorithms.
8. Describe the Linux implementation of user and programmer interfaces.

UNIT - 1 (12 hours)

OS objectives and functions: Multiprocessor system, Multiprogramming System, time sharing system.

Process description & control: Process, process states, creation & termination of processes, two & five model process model, processor modes, suspended process, process description, OS control structures, process control structures, process location, process attributes, process control , Threads overview, Multithreading modules Microkernels architecture and benefits.

CPU Scheduling: Basic concepts: CPU – I/O Burst Cycle, CPU Scheduler, Preemptive Scheduling, Dispatcher, Scheduling criteria, Scheduling Algorithms: FCFS, SJF, Priority, RR, Multilevel Queue Scheduling, Multilevel Feedback queue Scheduling, Algorithm Evaluation.

UNIT - 2 (12 hours)

Concurrency Control: Principles of concurrency, operating system concerns, process interaction, competition amongst processes for resources, cooperation amongst processes by sharing & communication.
Process Synchronization: Background, The Critical – Section Problem, Synchronization Hardware, Semaphores, classic problems of Synchronization: The Bounded Buffer Problem, the Readers-Writers Problem, The Dining-Philosophers Problem, Monitors.
Deadlocks: System model, deadlock characterization, methods for handling deadlocks, deadlock prevention, deadlock avoidance, deadlock detection, recovery from deadlock.

UNIT - 3 (12 hours)

Memory: Memory Hierarchy, Cache Memory.
Memory management: Address Binding, Logical vs Physical Address Space, Swapping, Contiguous Memory Allocation, Paging, Segmentation, Segmentation with paging.
Virtual Memory: Background, Demand Paging, Page Replacement: Basic Scheme, FIFO, Optimal, LRU, Allocation of frames, Thrashing: cause of Thrashing.
File Management: Files, File Management systems, file organization and access, file directories, file sharing, record blocking.

UNIT - 4 (12 hours)

Disk Scheduling & Management: Disk scheduling policies-FCFS, SSTF, SCAN, C-SCAN, LOOK , selection of a disk scheduling algorithm, Disk management, disk formatting, bad blocks.
The Linux Case Study: Design Principles, Kernel Modules, Process Management, Scheduling, Memory Management: Management of physical Memory, virtual memory, Execution and loading of user programs, Interprocess Communication.

Recommended Readings:

1. William Stallings; Operating Systems: Internal & design principles, 6th Edition; PHI.
2. A. Silberschatz, P. Galvin, G. Gagne; Operating systems Concepts, 6th Edition, John Wiley & Sons Pte. Ltd.
3. Andrew S. Tanenbaum; Modern Operating Systems, 2nd Edition; Pearson education
4. D.M. Dhamdhere; Operating Systems: A concept based approach; TataMc Graw Hill
5. Milan Milenkovic; Operating Systems: Concepts and design; TataMcGraw Hill

ETC/ECE 6.6 COMMUNICATION NETWORKS

Subject Code	Name of the Subject	Scheme of Instruction Hrs/Week			Scheme of Examination						
		L	T	P	Th Duration (Hrs)	Marks					
						Th	S	TW	O	P	Total
ETC/ECE 6.6	Communication Networks	3	1	2	3	100	25	--	--	25	150

Course Objectives:

The subject aims to provide the student with:

1. An introduction to the layered architecture of OSI model.
2. An understanding of the functions of the data link layer and its protocols.
3. An introduction to the network and transport protocols.
4. An introduction to various networking and internetworking devices and protocols used in application layer.

Course Outcomes:

The student after undergoing this course will be able to:

1. Explain the functions of the various layers of OSI model.
2. Implement the various line coding techniques.
3. Explain the various flow and error control techniques.
4. Design a multistage switch as well as distinguish between various switching techniques like Datagram approach, SVC, PVC.
5. Compare the data link protocols like HDLC, BISYNC, X.25 with respect to their working, frame formats and their applications.
6. Explain the need for internet protocols, routing algorithms and tackling the various problems which may occur in data networks.
7. Explain the various devices like repeaters, bridges, routers, firewalls with respect to real life examples.
8. Explain the application and working of ATM, ISDN and other protocols used at application layer.

UNIT - 1 (12 hours)

OSI Model: Layered architecture of OSI model, other layered architecture (TCP/IP).

Data communication concepts: parallel and serial transmission, asynchronous and synchronous transmission, line coding-NRZ, RZ, AMI, HDB3, B8ZS, Block Codes

Characteristics of transmission lines in time domain, crosstalk.

Modems: Types of modems, scrambler and descrambler, block schematic of modem network architecture.

LAN systems: Architecture: bus, ring, tree, star, wireless Ethernet, fast Ethernet, token ring, FDDI, Bluetooth, wireless LAN. Ethernet: Contention access, CSMA, CSMA/CD
Physical Layer: Interface-RS232, DTE-DCE interface, specifications, Null Modems.

UNIT - 2 (12 hours)

Data Link Layer: Frame design consideration, flow control, error control (stop and wait mechanism, sliding window), sequence numbering of frames, piggybacking acknowledgement, applications of data link protocols.
Data link protocols: BISYNC, transmission frames, protocol operation, HDLC, flow and error control in HDLC, framing in HDLC, transparency in HDLC, HDLC protocol operations, comparison of BISYNC and HDLC.
Switching: Switching networks, Circuits Switching, Space Division Switching, Time Division Switching, Packet Switching (datagram and virtual circuit [SVC, PVC]), Message Switching.
X.25 protocol: X.25 layers, characteristics of X.25 packet format, X.25 operation.

UNIT - 3 (12 hours)

Network Layer: Services, virtual circuits and datagram subnet, routing algorithms (shortest path, flooding, flow based, distance vector, link state), congestion control, choke packets, load shedding, jitter control, flow specifications, traffic shaping (leaky bucket and token bucket algorithm).
Internet protocols: IP protocols, addresses, internet control protocols, OSPF, BGP, mobile IP, IPV6.
Transport protocols: services, address, establishment of connection, releasing a connection, multiplexing, flow control and recovery, crash recovery, internet transport protocols (TCP and UOP), TCP protocol, TCP header, connection management, TCP congestion control, TCP transmission policy, timer management.

UNIT - 4 (12 hours)

Networking Devices: Repeaters, Bridges, Routers, Firewall.
ATM: ATM architecture- virtual connection, identifiers, cells, connection establishment and release.
ISDN: IDN,ISDN,ISDN channels(B,D,H), ISDN interfaces, functional groupings, ISDN protocols architecture-physical layer, data link layer, network layer, ISDN addressing, broadband ISDN.
Application Layer: DNS, DHCP, TFTP, Telnet, FTP, electronic mail, HTTP.

Recommended Readings:

1. Behrouz A. Forouzan; Data Communication & Networking, 2nd edition; Tata Mc-Graw Hill
2. Prakash C. Gupta; Data Communication and computer networks; PHI
3. William Stalling; Data & Computer Communications, 5th edition; PHI

4. Achyut S Godbole; Data Communication and Networks; Tata McGraw.
5. Andrew S. Tanenbaum; Computer Networks; PHI

List of Experiments:

(At least 8 experiments should be conducted from the list of experiments.)

1. To write and execute program for NRZ-L code.
2. To write and execute program for NRZ-I code.
3. To write and execute program for RZ code.
4. To write and execute program for Manchester Coding.
5. To write and execute program for Differential Manchester Coding.
6. To share data/files between two PC's within same or different network.
7. To create a VLAN in a switch and transfer one port at a time, and verify its functionality.
8. To create a VLAN in a switch and transfer range of ports in it, and verify its functionality.
9. To connect two switches together by trunking to transfer data.
10. To transfer data between two different networks using Routers.